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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte REIDAR LINDSTEDT

Appeal 2008-3837
Application 10/788,805
Technology Center 2800

Decided: September 29, 2008

Before CHARLES F. WARREN, PETER F. KRATZ, and
ROMULO H. DELMENDO, *Administrative Patent Judges*.

DELMENDO, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from a final rejection of all pending claims 1-7, 9-13, and 20-27. (Appeal Brief filed December 19, 2006; Final Office Action entered February 24, 2006). We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

Appellant's invention relates to a "semiconductor chip arrangement." (Spec. ¶ 0001).

Claims 1, 3-5, 7, 9, 11, 20, 22, 24, and 27 read as follows:

1. A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate including at least one interconnect formed on the first semiconductor substrate and also including at least one contact area that is electrically connected to the interconnect and is arranged on a side surface of the first semiconductor substrate; and

a second semiconductor substrate having at least one interconnect formed on the second semiconductor substrate and also including at least one contact area that is electrically connected to the interconnect and is arranged on a side surface of the second semiconductor substrate;

wherein the second semiconductor substrate is arranged on the first semiconductor substrate and the first semiconductor substrate is arranged on the mount element such that a first main surface of the second semiconductor substrate rests on the first semiconductor substrate, and a first main surface of the first semiconductor substrate rests on the mount element, and wherein an electrical contact is produced between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate and wherein the first and second semiconductor substrates each comprise an unpackaged semiconductor chip with integrated circuitry disposed therein.

3. The semiconductor chip arrangement of claim 1 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

4. The semiconductor chip arrangement of claim 1 wherein the first main surface of the first semiconductor substrate is attached to the mount element.

5. The semiconductor chip arrangement of claim 1 wherein the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate each extend from the first main surface to a second main surface of the respective semiconductor substrate.

7. A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate arranged over a surface of the mount element, the first semiconductor substrate including at least one interconnect formed thereon, the first semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the first semiconductor substrate;

a second semiconductor substrate arranged over the surface of the mount element alongside the first semiconductor substrate, the second semiconductor substrate including at least one interconnect formed thereon, the second semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the second semiconductor substrate, the second semiconductor substrate arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate; and

a third semiconductor substrate arranged over the second semiconductor substrate, the third semiconductor substrate including at least one interconnect formed thereon, the third semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the third semiconductor substrate, the third semiconductor substrate arranged so that an electrical contact is produced between the contact area of the third semiconductor substrate and the contact area of the second semiconductor substrate;

wherein the first, second and third semiconductor substrates each comprise unpackaged semiconductor chips with integrated circuitry disposed in the area of a first main surface

such that the integrated circuit is electrically coupled to the interconnect, the first main surface being parallel to the surface of the mount element.

9. The semiconductor chip arrangement of claim 7 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

11. The semiconductor chip arrangement of claim 7 wherein the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrate.

20. A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate arranged over a surface of the mount element, the first semiconductor substrate including at least one interconnect formed thereon, the first semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the first semiconductor substrate; and

a second semiconductor substrate arranged over the surface of the mount element alongside the first semiconductor substrate, the second semiconductor substrate including at least one interconnect formed thereon, the second semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the second semiconductor substrate;

wherein the second semiconductor substrate is arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate; and

wherein the first, and second semiconductor substrates each comprise an unpackaged semiconductor substrate having integrated circuitry disposed in the area of a first main surface, the first main surface being parallel to the surface of the mount element.

22. The semiconductor chip arrangement of claim 20 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

24. The semiconductor chip arrangement of claim 20 wherein the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrates.

27. The semiconductor chip arrangement of claim 7, wherein the first semiconductor substrate arranged in direct contact with the surface of the mount element, the second semiconductor substrate arranged in direct contact with the surface of the mount element, and the third semiconductor substrate arranged in direct contact with the second semiconductor substrate.

The prior art references relied upon by the Examiner to reject the claims on appeal are:

Malba	U.S. 5,834,162	Nov. 10, 1998
Glenn	U.S. 6,518,659	Feb. 11, 2003

The following rejections are before us for review:

Claims 1-4 and 26[1] are rejected under 35 U.S.C. § 102(b) as anticipated by Malba.

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[1] Although the Examiner's Answer states claim 25, not claim 26, is rejected under 35 U.S.C. § 102(b) (Ans. 3), Appellant recognizes in the Grounds of Rejection to be Reviewed on Appeal section of the Brief that claim 26 is correctly rejected under 35 U.S.C. § 102(b) instead of claim 25. (Br. 6). In the Grounds of Rejection to be Reviewed on Appeal section of the Answer, the Examiner agrees with Appellant's statement of the grounds of rejection to be reviewed. (Ans. 2). Also, it is clear from the record that the Examiner rejected claim 26, not claim 25, under 35 U.S.C. § 102(b) because the

Claims 5-7, 9-13, 20-25, and 27 are rejected under 35 U.S.C. § 103(a) as unpatentable in view of the combined teachings of Malba and Glenn.

ISSUES

Has Appellant shown reversible error in the Examiner's finding that the subject matter of claims 1-4 and 26 are anticipated by Malba?

Has Appellant shown reversible error in the Examiner's determination that the subject matter of claims 5-7, 9-13, 20-25, and 27 would have been obvious to one of ordinary skill in the art in view of the combined teachings of Malba and Glenn?

FINDINGS OF FACT

The record supports the following findings of fact, as well as any other findings of fact discussed in this opinion, by at least a preponderance of the evidence.

1. Appellant's Figs. 1C, 2C, and 3B are reproduced below:

FIG 1C

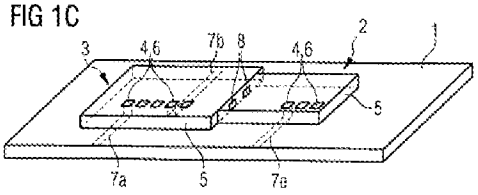
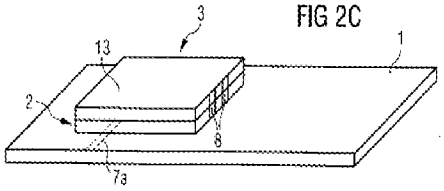
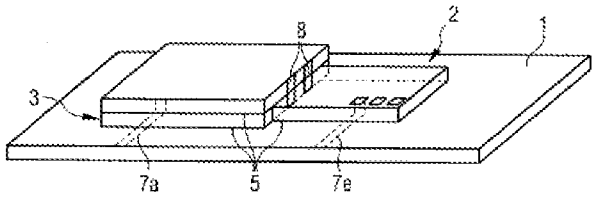


FIG 2C



Examiner discusses the subject matter of claim 26 in the rejection under 35 U.S.C. § 102(b) both in the Final Office Action (FAO) and the Answer. (FAO 3, ll. 14-16; Ans. 5, ll. 3-5). Appellant's acknowledgment of the correct listing of rejected claims in the Brief shows that Appellant was not prejudiced by this typographical error.

FIG 3B



Figs. 1C, 2C, and 3B depict different arrangements of semiconductor chips 2, 3, and 9 (unlabeled chip 9 is above chip 3 in Fig. 3B) on mount element 1 (side-by-side in Fig. 1C, top/bottom in Fig. 2C, and combined side-by-side and top/bottom in Fig. 3B), wherein the chips have lateral contact areas 8 arranged on their side surfaces for connecting to an adjacent chip. (Spec. ¶¶ 0037, 0042, and 0045-0047).

2. Appellants' Specification describes examples of ways in which semiconductor substrates may be fixed or attached to a mount element, but do not provide an explicit limiting definition for the claim term "attached." (Claim 4; Spec. ¶ 0023).

3. In the context of arranging structural parts, "attached" means "joined; connected; bound." (attached. Dictionary.com. *Dictionary.com Unabridged (v 1.1)*. Random House, Inc. (accessed: September 15, 2008) http://dictionary.reference.com/browse/attached).

4. Malba's Fig. 3 is reproduced below:

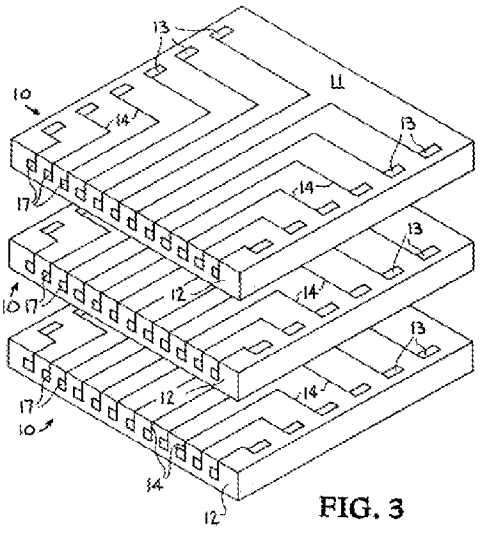


FIG. 3

Fig. 3 depicts an exploded view of three stacked integrated circuit chips 10 having top surface bond pads 13 extended via L-connects 14 to sidewall bond pads 17. (Col. 4, ll. 18-20).

5. Malba discloses a stack of integrated circuit chips having "bond pads on the sidewalls of the chips which enable ready access for interconnecting stacked chips or chip packages." (Col. 1, ll. 10-13).

6. Malba discloses "that when the chips 10 of FIG. 3 are stacked one on top of another electrical interconnects between the sidewall bond pads 17, or the interconnect portions on the sidewalls if bond pads are omitted, of the various chips can be easily made." (Emphasis omitted; col. 4, ll. 21-25; Fig. 3).

7. Electrical interconnections are necessarily made of conductive material.

8. Malba discloses:

> One solution to the demand for increased [chip packaging] density is to package the chips closer

> together, so that the effective density per unit volume increases. The densest packaging of chips is to stack them one on top of another into a single three dimensional (3D) unit or cube.

(Col. 1, ll. 27-31).

9. Malba discloses electrical interconnection configurations that "enable[] stacking of the chips, interconnection of the chip to other components, and/or packaging of stacked chips to other stacked chips or components." (Col. 5, ll. 54-56).

10. Glenn discloses stacking packages on top of each other to "allow[] an increase in the density of packages on a printed circuit board without a corresponding increase in the area of the printed circuit board consumed thereby." (Col. 1, ll. 40-42).

11. Glenn's Figs. 6B and 6D are reproduced below:

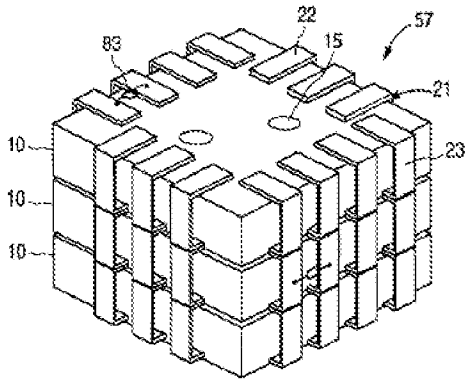


FIG. 6B

FIG. 6D

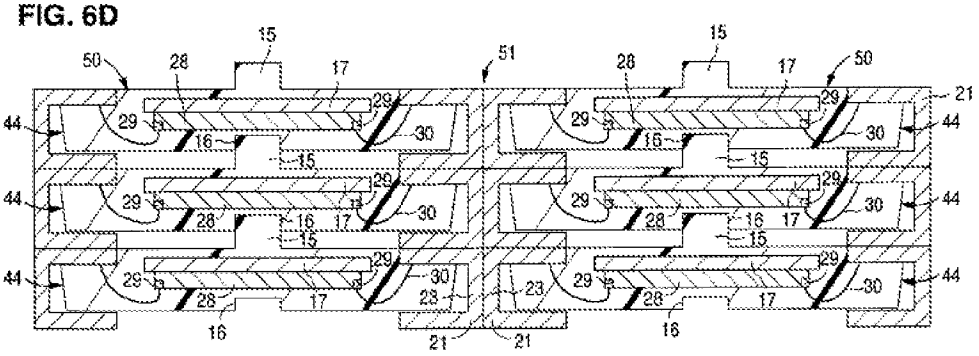


Fig. 6B depicts a stack 57 of three packaged semiconductors 10 having leads 21 with first portions 22 and second portions 23 for electrically interconnecting packages, where the leads extend from a first main surface to a second main surface of a package 10. (Col. 5, ll. 37-42). Fig. 6D depicts a double stack 51 of two stacks 50 of packages 44 that are electrically connected horizontally and vertically through leads 21, providing electrical interconnection of the integrated circuits 28 within the packages 44. (Col. 5, ll. 48-55).

12. Glenn describes:

> A plurality of such packages may be stacked one on top of the other so that the leads of a lower package will abut the leads of an upper package thereon. . . . Alternatively, one such package may be placed next to another on a printed circuit board so that the vertically extending portions of the leads of adjacent packages are juxtaposed for electrical interconnection.

(Col. 2, ll. 9-20)

13. Glenn discloses "[l]eads 21 may be plated with 80-20 solder for subsequent electrical connection of package 10 to a printed circuit board or to the leads of another package 10." (Emphasis omitted; Col. 4, ll. 1-3).

PRINCIPLES OF LAW

"To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently." *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997).

"[T]he PTO must give claims their broadest reasonable construction consistent with the specification. Therefore, we look to the specification to see if it provides a definition for claim terms, but otherwise apply a broad interpretation." *In re ICON Health and Fitness, Inc.*, 496 F.3d 1374, 1379 (Fed. Cir. 2007) (Citation omitted).

"The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1739 (2007).

ANALYSIS

Anticipation Rejection of Claims 1-4 in View of Malba

Appellant submits separate arguments with respect to claims 1, 3, and 4. We address these claims accordingly.

Claim 1

Appellant argues that Malba does not teach all limitations of claim 1 because the reference does not teach "an electrical contact between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate." (Br. 7, ll. 8-9). Appellant contends that although the electrical interconnects "could be between a first chip and a second chip, they could also be between the chips and a third component." (*Id.* 8, ll. 5-6).

The Examiner found that Malba teaches every limitation of the claimed invention. (Ans. 3-4; FF 4-6). In particular, the Examiner found "an electrical contact is produced between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate." (Ans. 4, ll. 11-12).

We agree with the Examiner. Although Malba discloses the interconnect can be between chips and other components in some embodiments, Malba also explicitly states "that when the chips . . . are stacked one on top of another electrical interconnects between the sidewall bond pads . . . of the various chips can be easily made." (FF 4, 9). In view of the description in the prior art, we find Appellant's arguments unpersuasive to show the Examiner erred in finding claim 1 anticipated by Malba.

Claim 3

In addition to the arguments made with regards to claim 1, Appellant contends: "Malba certainly does not teach . . . an electrical contact could be made with a conductive material applied between the contact areas as required by claim 3." (Br. 8, ll. 13-15).

For the same reason as discussed above with respect to claim 1, we do not agree with Appellant. Malba discloses an electrical connection between sidewall contacts of various ones of stacked integrated circuit chips. (FF 4-6, 9). Furthermore, the disclosed electrical connection would inherently be made with a "conductive material" (FF 7), as required by the claim. Here, again Appellant's arguments are unpersuasive in view of the teachings of the prior art.

Claim 4

While Appellant acknowledges that Malba discloses stacking unpackaged chips, Appellant contends that stacking "does not necessarily lead to the first main surface of one chip being *attached* to another chip." (Emphasis added; Br. 10, ll. 1-2). In support, Appellant directs us to the Specification for examples of the claimed structures:

> [T]he first semiconductor substrate may be fixed on the mount element by means of an adhesive or via electrical contacts, for example by means of soldered joints, or may be attached to the mount element by means of mechanical joints.

(*Id.* 10, ll. 3-6; Spec ¶ 0023). Appellant then asserts that "Malba teaches no such examples." (*Id.* 10, l. 6).

First, we look to construe the claim term "attached." Here, Appellant has not established an explicit definition of "attached" in the Specification. While the Specification provides examples of ways in which substrates *may* be fixed or attached to a mount element, these examples do not provide an explicit limiting definition. (FF 2). Additionally, none of these examples are recited in the claim. Accordingly, we give the claim term its broadest reasonable construction consistent with the Specification. *In re ICON Health and Fitness, Inc.* 496 F.3d at 1379. In the context of Appellant's invention, the ordinary meaning of "attached" is "joined[,] connected[, or] bound." (FF 3). Appellant has not directed us to any evidence that compels a contrary determination.

Here, the prior art discloses the claimed subject matter of a first semiconductor substrate that is "attached" to a mount element because Malba discloses a middle chip that is joined or bound by a lower chip (i.e., a mount element) when stacking, and is connected to the lower chip by an electrical connection between side contacts. (FF 4-6).

Thus, we find that Appellant has failed to show that the Examiner erred in finding claim 4 anticipated by Malba.

Obviousness Rejection of Claims 5-7, 9-13, 20-25, and 27 in View of Malba and Glenn

Appellant submits separate arguments with respect to claims 5, 7, 9, 11, 20, 22, 24, and 27. We address these claims accordingly.

Claim 5

Appellant asserts that "Malba does not teach that the contact area 17 extends from the first main surface to the second main surface." (Br. 10, ll. 14-15). Though acknowledging Glenn teaches "leads 21 [that] extend from a first main surface of the package to a second main surface of the package (*Id.* ll. 17-18), Appellant contends: "The contents of the two cited references do not provide any suggestion for combining their technical teaching since Glenn refers to a packaged semiconductor substrate surrounded by a housing and Malba refers to an unpackaged semiconductor substrate." (*Id.* ll. 20-22). Furthermore, Appellant argues "that one of ordinary skill in the art would not be able to use the leads of Glenn with the unpackaged semiconductor chips of Malba." (Br. 11, ll. 19-20). In particular, Appellant contends: "Glenn provides no teaching or suggestion that leads 21 could be formed by any method other than by packaging the integrated circuit 28." (*Id.* 12, ll. 5-6). Additionally, Appellant argues that "the configuration of leads taught by Glenn is incompatible with Malba's chip configuration" (*Id.* 12, ll. 14-15), because if Glenn's leads were used with the contacts of Malba, the contacts would be covered and "no longer readily available for attachment." (*Id.* 12, l. 13). Finally, in discussing the modification of Glenn's teachings,

Appellant argues that "[i]f it was obvious to apply Glenn's leads 21 to the unpackaged chip 28, Glenn would have done so." (Br. 13, ll. 2-3).

Appellant's arguments are unpersuasive. Malba states that "there is a demand for increased chip packaging density to increase performance, reduce space, and provide higher functionality per unit volume needed for applications." (Col. 1, ll. 22-24). Furthermore, Malba teaches:

> One solution to the demand for increased density is to package the chips closer together, so that the effective density per unit volume increases. The densest packaging of chips is to stack them one on top of another into a single three dimensional (3D) unit or cube.

(FF 8). Additionally, Malba discloses stacked chips can be electrically interconnected to other stacked chips. (FF 9).

Glenn teaches stacking packaged semiconductors having leads (i.e., contact areas) that extend from a first main surface to a second main surface to enable electrical connections between stacks and individual packaged semiconductors for increasing semiconductor density on a circuit board. (FF 10-13).

Thus, one of ordinary skill in the art would have found it obvious to modify the side contact areas in the semiconductor chips disclosed by Malba, by extending them from one main surface to another main surface to facilitate forming electrical interconnections between adjacent individual chips and chip stacks, thereby achieving a high density of electrically interconnected chips.

Furthermore, the side leads or contacts extending from one main surface to another main surface would have been understood by one of

ordinary skill in the art to predictably function as electrical interconnections in the claimed invention as they function in the prior art device.

Appellant has not provided persuasive evidence or reasoning to show that combining elements taught by Malba and Glenn is more than using known methods to achieve predictable results, or that the combination of the prior art techniques would not be successful because their application is beyond the skill of one of ordinary skill in the art. *KSR*, 127 S.Ct. at 1739. ("[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.").

Accordingly, Appellant has not shown that the Examiner erred in determining claim 5 obvious in view of the prior art.

Claim 7

Appellant relies on the same arguments as discussed above with respect to claims 1 and 5 and also contends: "Neither reference teaches or suggests a mount element with two substrates arranged alongside one another." (Br. 13, ll. 11-13; 14, ll. 7-13, 17-18).

We do not agree with Appellant for the same reasons as discussed above with respect to claims 1 and 5, and because Glenn teaches a circuit board as a mount element for stacking semiconductors alongside one another with vertical and horizontal electrical interconnections between packages. (FF 4-6, 8-13).

As discussed above, Malba discloses that extending top bond pads to the chip sidewalls "enables stacking of the chips,

interconnection of the chip to other components, and/or packaging of stacked chips to other stacked chips or components. (FF 9).

Thus, combining Malba's teachings of interconnecting stacked unpackaged chips to other stacked unpackaged chips with Glenn's teachings of stacking semiconductor packaged chips arranged alongside each other on a mount element would have been obvious to one of ordinary skill in the art to obtain the predictable result of increasing chip density and memory density on a circuit board mount, regardless if the chips are packaged or unpackaged. *KSR*, 127 S.Ct. at 1739.

Here also, Appellant has not directed us to any persuasive evidence or reasoning that the use of a circuit board as a mount element with side by side stacking of unpackaged chips was beyond the skill of one of ordinary skill in the art, or that the prior art teaches away from the combination. (Br. 6-18).

We find Appellant has failed to show the Examiner erred in determining the subject matter of claim 7 would have been obvious in view of the prior art.

Claim 9

Appellant argues that Malba and Glenn do not teach or suggest the claimed limitation of "a conductive material applied between the contact area on the first semiconductor substrate and the contact area of the second semiconductor substrate." (Claim 9; Br. 15, ll. 12-15).

We do not agree. Glenn explicitly discloses that solder is plated on the contact area of the leads for electrical connection between leads. (FF 13). Therefore, Appellant has not shown the Examiner erred in determining claim 9 obvious in view of the prior art.

Claim 11

Appellant "submits that the references of record do not teach or suggest the limitations of claim 11" (Br. 16, ll. 4-5), and relies on the same arguments as discussed above with respect to claim 5:

> [I]t would not be obvious to process an unpackaged substrate in a manner taught for packaged chips. Further, doing so would eliminate the need for the sidewall pads 17 taught by Malba. If Malba could be used with the C-leads 21 taught by Glenn, the sidewall pads 17 would be rendered useless. Conversely, if Glenn could have used the C-leads on unpackaged chips, he would have done so because it further enhances his stated goal of maximizing density.

(Br. 16, ll. 6-11).

As discussed above, the combination of Malba's teaching of stacked unpackaged chips with sidewall contacts and Glenn's teachings of extending side contacts from a first main surface to a second main surface to facilitate making electrical connections between stacked packaged chips would have been obvious, as the combination merely combines familiar elements by known methods to achieve a predictable result. *KSR*, 127 S.Ct. at 1739. Appellant's arguments are unpersuasive for the same reasons as discussed above with respect to claim 5. Accordingly, Appellant has failed to show that the Examiner erred in determining claim 11 obvious in view of the prior art.

Claim 20

Appellant relies on the same arguments presented with respect to claim 7 that "the two references do not teach the limitations because 1) the references are not properly combinable and 2) neither reference teaches the mount element required by claim 20." (Br. 16, ll. 18-20).

Appellant's arguments are unpersuasive for the same reasons as discussed above with respect to claim 7. Therefore, we find that Appellant has not shown that the Examiner erred in determining the subject matter of claim 20 obvious in view of the prior art.

Claim 22

Appellant relies on the same arguments presented with respect to claim 9 and contends that the prior art does not teach or suggest "a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate." (Claim 22; Br. 17, ll. 1-5).

As discussed above with respect to claim 9, we do not agree. Glenn explicitly discloses that solder is plated on the contact area of the leads for electrical connection between leads. (FF 13). Therefore, Appellant's argument fails to show the Examiner erred in determining claim 22 obvious in view of the prior art.

Claim 24

Appellant relies on the same arguments presented with respect to claim 5:

> [I]t would not be obvious to process an unpackaged substrate in a manner taught for packaged chips. Further, doing so would eliminate the need for the sidewall pads 17 taught by Malba. If Malba could be used with the C-leads 21 taught by Glenn, the sidewall pads 17 would be rendered useless. Conversely, if Glenn could have used the C-leads on unpackaged chips, he would have done so because it further enhances his stated goal of maximizing density.

(Br. 17, l. 18 through 18, l. 2).

As discussed above, the combination of Malba's teachings of stacked semiconductor unpackaged chips and Glenn's teachings to extend side contacts from a first main surface to a second main surface would have been obvious to one of ordinary skill in the art, as the combination merely combines familiar elements by known methods to achieve a predictable result. *KSR*, 127 S.Ct. at 1739. Here again, Appellant's arguments are unpersuasive for the same reasons as discussed above with respect to claim 5. Accordingly, Appellant has failed to show that the Examiner erred in determining claim 24 obvious in view of the prior art.

Claim 27

Appellant argues that Malba and Glenn do not teach or suggest the limitations of "[c]laim 27 . . . [that] requires that 'the first semiconductor substrate arranged in direct contact with the surface of the mount element [and] the second semiconductor substrate [is] arranged in direct contact with the surface of the mount element.'" (Claim 27; Br. 18, ll. 5-8). Appellant contends that "[e]ven if these packages [disclosed by Glenn] are over a mount element, the semiconductor substrates are not in direct contact with a surface of the mount element." (Br. 18, ll. 12-13). Appellant argues that "the integrated circuit 28 of the middle package is never in direct contact with the package 10 beneath it." (*Id.* ll. 17-18).

Appellant's argument is unpersuasive. The dispositive question before us is whether it would have been obvious to one of ordinary skill in the art to arrange Malba's stacked unpackaged chips on a circuit board in the same arrangement taught by Glenn for packaged chips.

As instructed by *KSR*, "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would

improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *KSR*, 127 S.Ct. at 1739.

As discussed above, Malba discloses that the demand for increased chip density can be satisfied by electrically interconnecting stacked unpackaged chips, which is accomplished by placing electrical contacts on the sidewalls of the unpackaged chips to enable electrical connections between individual stacked chips and between stacks of chips. (FF 4, 5, 8, 9). Glenn teaches stacking packaged chips alongside each other directly on a circuit board to increase the packaged chip density on the circuit board. (FF 10-12). Thus, one of ordinary skill in the art would have understood to arrange Malba's stacked unpackaged chips directly on a circuit board as taught by Glenn to achieve increased chip density on a circuit board, regardless of whether the chips are unpackaged or packaged. Appellant has not directed us to any persuasive evidence or reasoning that the combination would have been beyond the skill of one of ordinary skill in the art.

For these reasons we find that Appellant has not shown that the Examiner erred in determining the subject matter of claim 27 obvious in view of the prior art.

CONCLUSION

Appellant has failed to show the Examiner reversibly erred in finding claims 1-4 and 26 anticipated by Malba.

Appellant has also failed to show that the Examiner reversibly erred in concluding that one of ordinary skill in the art would have found the subject

matter of appealed claims 5-7, 9-13, 20-25, and 27 obvious in view of the combined teachings of Malba and Glenn.

Accordingly, the decision of the Examiner to reject all the appealed claims is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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